| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 1 | 281 | instruction$1 with (add$3 or insert$3) with power | USPAT; US-PGPUB | 2002/09/17 11:59 |
| 4 | 21 | instruction$1 near3 (add$3 or insert$3) near2 power | USPAT; US-PGPUB | 2002/09/17 12:15 |
| 7 | 10 | instruction$1 near3 (add$3 or insert$3) near2 power | EPO; JPO; DERWENT; IBM_TDB | 2002/09/17 12:19 |
| 12 | 2323 | (power$3 adj2 off) near3 (device$1 or function$2 or drive$1) | EPO; JPO; DERWENT; IBM_TDB | 2002/09/17 12:41 |
| 22 | 0 | ((save$1 or saving$1 or reduce$1 or reducing or reduction$1) near3 ((power$3 adj2 off) near3 (device$1 or function$2 or drive$1))) and (instruction$1 near3 (add$3 or insert$3) near2 power) | EPO; JPO; DERWENT; IBM_TDB | 2002/09/17 12:23 |
| 17 | 55 | (save$1 or saving$1 or reduce$1 or reducing or reduction$1) near3 ((power$3 adj2 off) near3 (device$1 or function$2 or drive$1)) | EPO; JPO; DERWENT; IBM_TDB | 2002/09/17 12:42 |
| 27 | 0 | (save$1 or saving$1 or reduce$1 or reducing or reduction$1) near3 ((power$3 adj2 off) near3 (device$1 or function$2 or drive$1)) | USPAT; US-PGPUB | 2002/09/17 12:41 |
| 30 | 5132 | (power$3 adj2 off) near3 (device$1 or function$2 or drive$1) | USPAT; US-PGPUB | 2002/09/17 12:42 |
| 36 | 1 | (instruction$1 with (add$3 or insert$3) with power) and ((save$1 or saving$1 or reduce$1 or reducing or reduction$1) near3 ((power$3 adj2 off) near3 (device$1 or function$2 or drive$1))) | USPAT; US-PGPUB | 2002/09/17 13:22 |
| 33 | 78 | (save$1 or saving$1 or reduce$1 or reducing or reduction$1) near3 ((power$3 adj2 off) near3 (device$1 or function$2 or drive$1)) | USPAT; US-PGPUB | 2002/09/17 12:50 |

09/285,879

| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 1 | 281 | instruction$1 with (add$3 or insert$3) with power | USPAT; US-PGPUB | 2002/09/17 11:59 |
| 4 | 21 | instruction$1 near3 (add$3 or insert$3) near2 power | USPAT; US-PGPUB | 2002/09/17 12:15 |
| 7 | 10 | instruction$1 near3 (add$3 or insert$3) near2 power | EPO; JPO; DERWENT; IBM_TDB | 2002/09/17 12:15 |

US-PAT-NO: 6307281
DOCUMENT-IDENTIFIER: US 6307281 B1

TITLE: System and method for reducing power dissipation in a circuit

DATE-ISSUED: October 23, 2001

INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---|---|---|---|---|
| Houston; Theodore W. | Richardson | TX | N/A | N/A |

US-CL-CURRENT: 307/31; 307/39

ABSTRACT:

A method for selective allocation of power to elements of a circuit comprises identifying at least one element of the circuit for reduced power dissipation and selecting the at least one element. The method further comprises altering an input to the at least one element thereby reducing the power dissipated by the at least one element.

26 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

---------- KWIC ---------

Detailed Description Text - DETX:

The present invention contemplates several embodiments directed towards determining when a specific element 36 of execution unit 34 will be selected for reduced power dissipation via selection signal 35. In one embodiment of the present invention, logic component 32 sends a selection signal 35 to a specific element 36 based on a power down instruction handled and forwarded by instruction handler 30. The power down instruction may specify a particular element 36 to be powered down. The term powered down means that element 36 shall operate in a mode whereby less power is dissipated by element 36, hereinafter sometimes referred to as a reduced power dissipation mode. The **power down instruction may be inserted** into executable code by a specialized process of a compiler or assembler in response to examining coded instructions and determining intervals in which a specific element will be inactive during execution. Such a process would **insert power down instructions** at the beginning of the interval of inactivity and insert related power up instructions when such intervals expire.

US-PAT-NO: 5790877
DOCUMENT-IDENTIFIER: US 5790877 A

TITLE: Method for controlling a processor for power-saving in a computer for executing a program, compiler medium and processor system

DATE-ISSUED: August 4, 1998


INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---|---|---|---|---|
| Nishiyama; Hiroyasu | Kawasaki | N/A | N/A | JP |
| Kikuchi; Sumio | Machida | N/A | N/A | JP |
| Mori; Noriyasu | Kawasaki | N/A | N/A | JP |
| Nishimoto; Akira | Kawasaki | N/A | N/A | JP |
| Takeuchi; Yooichi | Kawasaki | N/A | N/A | JP |


US-CL-CURRENT: 713/323; 713/320 ; 713/321 ; 713/322 ; 713/324


ABSTRACT:

In a processor system including a plurality of hardware resources, a method for arranging a program to suppress the power consumption by the resources includes the steps of determining which ones of the hardware resources are to be operated and from which instruction cycle to which instruction cycle to execute each instruction of the program; and based on the determination, adding an instruction to lower frequencies of clock signals inputted to the hardware resources and an instruction to restore the frequency at positions adjacent to the beginning and the end of the period during which the hardware resources are not operated and compiling the program. The processor system decodes the compiled program and lowers the frequency of the clock signal inputted to the hardware resources in accordance with the frequency lowering instruction and the frequency restoring instruction detected in the decoding step. The clock signals sent to the hardware resources are stopped by the frequency lowering instruction to the resource of the hardware resources for which the clock frequency may be lowered to zero.


17 Claims, 12 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 6

---------- KWIC ---------

Detailed Description Text - DETX:

In the process of the clock control instruction insertion unit 502, the clock control **instruction is inserted to reduce the power** consumption by the non-used hardware resources as much as possible. In some cases, the number of execution cycles may increase by the insertion of the clock control instruction due to the limitation of the simultaneously executed respectively in a plurality of processors. In such a case, when the clock control instruction is inserted in the step 805 of FIG. 8, whether the number of cycles increases or not may be checked in the step 804.

CLIPPEDIMAGE= JP359009729A

PAT-NO: JP359009729A

DOCUMENT-IDENTIFIER: JP 59009729 A

TITLE: SEMICONDUCTOR DEVICE

PUBN-DATE: January 19, 1984

INVENTOR-INFORMATION:
NAME
UMEKI, TSUNENORI

ASSIGNEE-INFORMATION:

| NAME | COUNTRY |
| --- | --- |
| MITSUBISHI ELECTRIC CORP | N/A |

APPL-NO: JP57119365

APPL-DATE: July 7, 1982

INT-CL (IPC): G06F001/00;H01L027/04

ABSTRACT:

PURPOSE: To minimize heat generation of an integrated circuit and **power consumption, by adding an instruction** for turning on and off supply power in block unit of function blocks which operate independently from each other, to an instruction processed by a processor.

CONSTITUTION: In a processor 1b, when electric power is inputted to a power supply pad and a power supply line 2, and a prescribed resetting signal and a clock signal are inputted to each processor 1b. A power cut block 7 on each function block 6 sets a power state latch 9 to a specified state by a power state resetting signal 10. Subsequently, an instruction inputted from an instruction bus 3 is decoded by a decoder 4, and in case when its contents are an instruction for changing turn-on and turn-off of power in some function block 6, a power state changing signal 11 is outputted to the latch 9 from an internal control part 5, and power of the designated function block is turned on or off.

CLIPPEDIMAGE= JP411085347A

PAT-NO: JP411085347A

DOCUMENT-IDENTIFIER: JP 11085347 A

TITLE: ELECTRIC COMPONENT MOUNT BOARD

PUBN-DATE: March 30, 1999

INVENTOR-INFORMATION:
NAME
MATSUMURA, TORU

ASSIGNEE-INFORMATION:

| NAME | COUNTRY |
|---|---|
| HITACHI LTD | N/A |

APPL-NO: JP09246423

APPL-DATE: September 11, 1997

INT-CL (IPC): G06F003/00;G06F001/26

ABSTRACT:

PROBLEM TO BE SOLVED: To cut the power supply to unused functions among **functions and to save the electric power by turning on and off** an input/output interface circuit according to the attachment/detachment signal of a connector.

SOLUTION: When a connector 37 connected to an external auxiliary device is connected to an input/output terminal 10 and brought into mechanical or electric contact with an adjacent switch 24, a switch 24 sends a signal indicating the connection with the connector 37. A power source controller 23 receives the signal and connects the power source 38 from a personal computer 5 to the input/output interface circuit 2. When the power source of the input/output interface circuit 2 is turned on, the CPU 16 in the personal computer 5 performs actuating operation. The actuating operation can be performed by, for example, the operating system of the personal computer 5 and even when the input/output interface circuit 2 is powered OFF, the CPU 16 in the personal computer 5 can perform ending operation.

DERWENT-ACC-NO: 1999-414146
DERWENT-WEEK: 199935


TITLE: Integrated power supply switching control system in information processor - has internal power supply switches connected to each functional group, which are selectively switched ON or OFF by controller, so that power is supplied only to the necessary functional group

PATENT-ASSIGNEE: MATSUSHITA DENKI SANGYO KK[MATU]

PRIORITY-DATA: 1997JP-0333865 (December 4, 1997)

PATENT-FAMILY:

| PUB-NO | PUB-DATE | LANGUAGE | PAGES | MAIN-IPC |
|---|---|---|---|---|
| JP 11167439 A | June 22, 1999 | N/A | 005 | G06F 001/26 |

APPLICATION-DATA:

| PUB-NO | APPL-DESCRIPTOR | APPL-NO | APPL-DATE |
|---|---|---|---|
| JP11167439A | N/A | 1997JP-0333865 | December 4, 1997 |

INT-CL (IPC): G06F001/26; G06F001/32 ; G06F015/02

ABSTRACTED-PUB-NO: JP11167439A
BASIC-ABSTRACT: NOVELTY - Independent internal power supply switches (2-4) are connected to each group which are selectively turned ON-OFF by a controller (1), so that power supply is selectively fed only to the required peripherals.
DETAILED DESCRIPTION - Components of an information processor are divided into several groups comprising CPU (5) and main memory (6) under a group, modem (7) in next group and display device (8), keyboard (9) forming another group.

USE - In information processor for selectively turning ON or OFF of peripheral units.

ADVANTAGE - Enables **saving of electrical power by turning off unnecessary functional** units. Offers low cost and reliable power control system.
DESCRIPTION OF DRAWING(S) - The diagram shows the block diagram of the information processor with built-in power supply control system. (1) Controller; (2-4) Power supply switches; (5) CPU; (6) Main memory; (7) Modem; (8) Display device; (9) Keyboard.

CHOSEN-DRAWING: Dwg.1/2

TITLE-TERMS:
INTEGRATE POWER SUPPLY SWITCH CONTROL SYSTEM INFORMATION PROCESSOR INTERNAL POWER SUPPLY SWITCH CONNECT FUNCTION GROUP SELECT SWITCH CONTROL SO POWER SUPPLY NECESSARY FUNCTION GROUP

DERWENT-CLASS: T01

EPI-CODES: T01-J01; T01-L01;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1999-310239

DERWENT-ACC-NO: 1999-414146
DERWENT-WEEK: 199935


TITLE: Integrated power supply switching control system in information processor - has internal power supply switches connected to each functional group, which are selectively switched ON or OFF by controller, so that power is supplied only to the necessary functional group

PATENT-ASSIGNEE: MATSUSHITA DENKI SANGYO KK[MATU]

PRIORITY-DATA: 1997JP-0333865 (December 4, 1997)

PATENT-FAMILY:

| PUB-NO | PUB-DATE | LANGUAGE | PAGES | MAIN-IPC |
|---|---|---|---|---|
| JP 11167439 A | June 22, 1999 | N/A | 005 | G06F 001/26 |

APPLICATION-DATA:

| PUB-NO | APPL-DESCRIPTOR | APPL-NO | APPL-DATE |
|---|---|---|---|
| JP11167439A | N/A | 1997JP-0333865 | December 4, 1997 |

INT-CL (IPC): G06F001/26; G06F001/32 ; G06F015/02

ABSTRACTED-PUB-NO: JP11167439A
BASIC-ABSTRACT: NOVELTY - Independent internal power supply switches (2-4) are connected to each group which are selectively turned ON-OFF by a controller (1), so that power supply is selectively fed only to the required peripherals.
DETAILED DESCRIPTION - Components of an information processor are divided into several groups comprising CPU (5) and main memory (6) under a group, modem (7) in next group and display device (8), keyboard (9) forming another group.

USE - In information processor for selectively turning ON or OFF of peripheral units.

ADVANTAGE - Enables **saving of electrical power by turning off unnecessary functional** units. Offers low cost and reliable power control system.
DESCRIPTION OF DRAWING(S) - The diagram shows the block diagram of the information processor with built-in power supply control system. (1) Controller; (2-4) Power supply switches; (5) CPU; (6) Main memory; (7) Modem; (8) Display device; (9) Keyboard.

CHOSEN-DRAWING: Dwg.1/2

TITLE-TERMS:
INTEGRATE POWER SUPPLY SWITCH CONTROL SYSTEM INFORMATION PROCESSOR INTERNAL POWER SUPPLY SWITCH CONNECT FUNCTION GROUP SELECT SWITCH CONTROL SO POWER SUPPLY NECESSARY FUNCTION GROUP

DERWENT-CLASS: T01

EPI-CODES: T01-J01; T01-L01;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1999-310239

DERWENT-ACC-NO: 1997-259198
DERWENT-WEEK: 200207


TITLE: Computer peripheral with low power standby apparatus - includes signal generator which sends power management commands to peripheral device after passage of pre=stored time period of computer inactivity

INVENTOR: DORNIER, P; KIKINIS, D

PATENT-ASSIGNEE: ELONEX TECHNOLOGIES INC[ELONN], ELONEX IP HOLDINGS LTD[ELONN]

PRIORITY-DATA: 1995US-0548662 (October 26, 1995) , 1992US-0940688 (September 4, 1992) , 1992US-0984370 (December 2, 1992) , 1993US-0141413 (October 22, 1993) , 1993US-0175743 (December 30, 1993) , 1994US-0319256 (October 6, 1994) , 1998US-0066098 (April 23, 1998)

PATENT-FAMILY:

| PUB-NO | PUB-DATE | LANGUAGE | PAGES | MAIN-IPC |
|---|---|---|---|---|
| JP 3249824 B2 | January 21, 2002 | N/A | 015 | G06F 001/26 |
| WO 9715913 A1 | May 1, 1997 | E | 030 | G09G 005/00 |
| US 5821924 A | October 13, 1998 | N/A | 000 | G09G 005/00 |
| JP 10512382 W | November 24, 1998 | N/A | 030 | G06F 001/26 |
| US 5919263 A | July 6, 1999 | N/A | 000 | G06F 013/00 |

DESIGNATED-STATES: CN JP AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE

CITED-DOCUMENTS: 1.Jnl.Ref; JP 2024696 ; US 4806784 ; US 5167024

APPLICATION-DATA:

| PUB-NO | APPL-DESCRIPTOR | APPL-NO | APPL-DATE |
|---|---|---|---|
| JP 3249824B2 | N/A | 1996WO-US17109 | October 24, 1996 |
| JP 3249824B2 | N/A | 1997JP-0516798 | October 24, 1996 |
| JP 3249824B2 | Previous Publ. | JP 10512382 | N/A |
| JP 3249824B2 | Based on | WO 9715913 | N/A |
| WO 9715913A1 | N/A | 1996WO-US17109 | October 24, 1996 |
| US 5821924A | Cont of | 1992US-0940688 | September 4, 1992 |
| US 5821924A | Cont of | 1992US-0984370 | December 2, 1992 |
| US 5821924A | Cont of | 1993US-0141413 | October 22, 1993 |
| US 5821924A | CIP of | 1993US-0175743 | December 30, 1993 |
| US 5821924A | CIP of | 1994US-0319256 | October 6, 1994 |
| US 5821924A | N/A | 1995US-0548662 | October 26, 1995 |
| US 5821924A | Cont of | US 5321428 | N/A |
| US 5821924A | Cont of | US 5389952 | N/A |
| US 5821924A | CIP of | US 5489935 | N/A |
| JP 10512382W | N/A | 1996WO-US17109 | October 24, |

| | | | |
|---|---|---|---|
| 1996 | | | |
| JP 10512382W | N/A | 1997JP-0516798 | October 24, |
| 1996 | | | |
| JP 10512382W | Based on | WO 9715913 | N/A |
| US 5919263A | Cont of | 1992US-0940688 | September 4, |
| 1992 | | | |
| US 5919263A | Cont of | 1992US-0984370 | December 2, |
| 1992 | | | |
| US 5919263A | Cont of | 1993US-0141413 | October 22, |
| 1993 | | | |
| US 5919263A | CIP of | 1993US-0175743 | December 30, |
| 1993 | | | |
| US 5919263A | CIP of | 1994US-0319256 | October 6, 1994 |
| US 5919263A | Div ex | 1995US-0548662 | October 26, |
| 1995 | | | |
| US 5919263A | N/A | 1998US-0066098 | April 23, 1998 |
| US 5919263A | Cont of | US 5321428 | N/A |
| US 5919263A | Cont of | US 5389952 | N/A |
| US 5919263A | CIP of | US 5489935 | N/A |
| US 5919263A | Div ex | US 5821924 | N/A |

INT-CL (IPC): G06F001/26; G06F001/32 ; G06F013/00 ; G09G005/00 ; G09G005/12 ; H04N005/63

RELATED-ACC-NO: 1994-101324;1994-200495 ;1995-246486

ABSTRACTED-PUB-NO: US 5821924A
BASIC-ABSTRACT: The computer system includes a host computer with a CPU, a memory and an input apparatus, and a connected peripheral device (347). It also has a power management mechanism for managing power usage by the peripheral device. A timer detects periods of inactivity at the computer. A signal generator generates power management commands for the peripheral device.

A power manager circuit is contained in the peripheral device. After the passage of a pre-stored time period of inactivity of the host computer, the timer signals the signal generator to send a power management command to the peripheral device. The power management circuit causes the peripheral **device to assume a reduced power state other than off** in response to the command.

USE - Relates to field of auto power saving methods and in particular to reduction of power used by peripheral device when not in use by computer.

ABSTRACTED-PUB-NO: US 5919263A
EQUIVALENT-ABSTRACTS: The computer system includes a host computer with a CPU, a memory and an input apparatus, and a connected peripheral device (347). It also has a power management mechanism for managing power usage by the peripheral device. A timer detects periods of inactivity at the computer. A signal generator generates power management commands for the peripheral device.

A power manager circuit is contained in the peripheral device. After the passage of a pre-stored time period of inactivity of the host computer, the timer signals the signal generator to send a power management command to the peripheral device. The power management circuit causes the peripheral **device to assume a reduced power state other than off** in response to the command.

USE - Relates to field of auto power saving methods and in particular to reduction of power used by peripheral device when not in use by computer.

The computer system includes a host computer with a CPU, a memory and an input apparatus, and a connected peripheral device (347). It also has a power management mechanism for managing power usage by the peripheral device. A timer detects periods of inactivity at the computer. A signal generator generates power management commands for the peripheral device.

A power manager circuit is contained in the peripheral device. After the passage of a pre-stored time period of inactivity of the host computer, the timer signals the signal generator to send a power management command to the peripheral device. The power management circuit causes the peripheral **device to assume a reduced power state other than off** in response to the command.

USE - Relates to field of auto power saving methods and in particular to reduction of power used by peripheral device when not in use by computer.

WO 9715913A

CHOSEN-DRAWING: Dwg.3/8

TITLE-TERMS:
COMPUTER PERIPHERAL LOW POWER STANDBY APPARATUS SIGNAL GENERATOR SEND POWER MANAGEMENT COMMAND PERIPHERAL DEVICE AFTER PASSAGE TIME PERIOD COMPUTER INACTIVE

DERWENT-CLASS: P85 T01 T04 U24

EPI-CODES: T01-H05A; T01-L01; T04-H; U24-X;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1997-214288

US-PAT-NO: 5954820
DOCUMENT-IDENTIFIER: US 5954820 A

TITLE: Portable computer with adaptive demand-driven power management

DATE-ISSUED: September 21, 1999

INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---|---|---|---|---|
| Hetzler; Steven Robert | Los Altos | CA | N/A | N/A |


US-CL-CURRENT: 713/323; 713/324

ABSTRACT:

A method for managing power in a portable computer uses past access history of the various electrically-powered computer components and a prediction of future user demands to determine power-save mode entry and exit conditions. The component or the computer system keeps track of the access patterns. In the case of the display system component, such as the LCD display panel, because the access occurs when the user is watching the display panel and is thus not possible to measure directly, the accesses are measured indirectly from keyboard and/or pointing device activity. Each component access is detected and used to compute a current access frequency. The current access frequency is compared to a previously calculated and continuously updated threshold frequency. The threshold frequency is representative of the access pattern, e.g., uniform or sporadic, and is computed from equations that include adjustable gain factors. During operation of the component the appropriate power-save mode is entered when the current access frequency falls below the threshold frequency. The component can also adapt dynamically to varying workload situations, thereby saving more energy without degrading performance. This is accomplished by adjusting the gain factors parameters in response to tracking the actual performance of the system, thereby changing the threshold frequency. The component also determines when to exit a power-save mode without necessarily waiting for a user access.

31 Claims, 12 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 12

---------- KWIC ---------

Detailed Description Text - DETX:

The above description specifically describes the application of the invention to optical storage devices, such as CD-ROM and DVD drives, and to the LCD display subsystem. However, the invention is equally applicable to any component of the mobile computer, which has component accesses which can be measured directly (as for the CD-ROM drive), or indirectly (as for the LCD panel). For example, the power management of the LCD panel can be extended to place the entire computer in a deeper power-save mode, such as STANDBY. (Most mobile computers have a STANDBY power-**save mode, where the storage devices are powered off** in addition to the LCD panel being powered off). This would be accomplished by defining a second power-save mode for the LCD display, in addition to LCD OFF. The STANDBY mode would have a larger timing window, and

be tuned as described above. Further modes, such as SUSPEND (where the CPU and other peripherals are essentially turned off, and power is used only to retain the RAM and registers, and detect the user command to exit SUSPEND) and HIBERNATE (where the RAM and register contents are written to the hard disk, and the entire system powered off) can be added similarly. Also, any of the other components shown in FIG. 1 which have power-save modes, can use the present invention to manage the usage of the power-save modes. All components have at least two modes of operation, an ACTIVE mode which is typically the full operational mode, and at least one less than full operation or reduced-power mode, which is typically the OFF mode. Many have more modes, such as a reduced clock rate mode for the CPU 4, and a SUSPEND mode for the modem and Ethernet adapter. Each of these modes may be characterized for its energy and performance behavior as described above. Some will behave like the CD-ROM drive 15, with a different amount of power depending on how active the component is, while others will behave more like the LCD display panel. For many components, such as communications devices 18 (modems, Ethernet adapters), and the CPU 4, it is possible to measure the access to the component itself. For others, it may be better to measure the accesses indirectly through another component. For example, the audio controller 20 is best handled by using the keyboard and pointer activity to measure accesses, like the LCD display. It should be apparent to one skilled in the art how to apply this invention to any such component or subsystem in a computer.

US-PAT-NO: 5919263
DOCUMENT-IDENTIFIER: US 5919263 A

TITLE: Computer peripherals low-power-consumption standby system

DATE-ISSUED: July 6, 1999


INVENTOR-INFORMATION:

| NAME | CITY | STATE | ZIP CODE | COUNTRY |
|---|---|---|---|---|
| Kikinis; Dan | Saratoga | CA | N/A | N/A |
| Dornier; Pascal | Sunnyvale | CA | N/A | N/A |


US-CL-CURRENT: 713/320; 713/300


ABSTRACT:

A system for reducing power consumption of a computer peripheral device connected to a host computer during periods of inactivity of the host computer has a dedicated input for initiating power management operations. When the dedicated input is sensed a timer is started and a power management command is sent to the peripheral **device, initiating a reduced-power mode other than off**. In a preferred embodiment the system also starts a timer when the dedicated input is sensed, and after a predetermined time a second power management command is sent triggering a second reduced-power mode for the peripheral. The system is adapted to peripheral devices such as video displays and printers.


14 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 9

---------- KWIC ---------

Abstract Text - ABTX:


A system for reducing power consumption of a computer peripheral device connected to a host computer during periods of inactivity of the host computer has a dedicated input for initiating power management operations. When the dedicated input is sensed a timer is started and a power management command is sent to the peripheral **device, initiating a reduced-power mode other than off**. In a preferred embodiment the system also starts a timer when the dedicated input is sensed, and after a predetermined time a second power management command is sent triggering a second reduced-power mode for the peripheral. The system is adapted to peripheral devices such as video displays and printers.


Brief Summary Text - BSTX:

In a computer system having a host computer with a central processing unit (CPU), a memory, and input apparatus, and having also a connected peripheral device, a power management system for managing power usage by the peripheral device, the power management system comprising a user input dedicated to triggering a power-management routine; a signal generator for generating at least one power-management command for the peripheral device; and a power manager circuit in the peripheral device. In this system activation of the dedicated user input causes the signal generator to send a power management

command to the peripheral device, and the power manager circuit in the peripheral device causes the peripheral **device to assume a reduced-power state other than off** in response to the power management command.

Claims Text - CLTX:

wherein activation of the dedicated user input causes the signal generator to send a power management command to the peripheral device, and the power manager circuit in the peripheral device causes the peripheral **device to assume a reduced-power state other than off** in response to the power management command.